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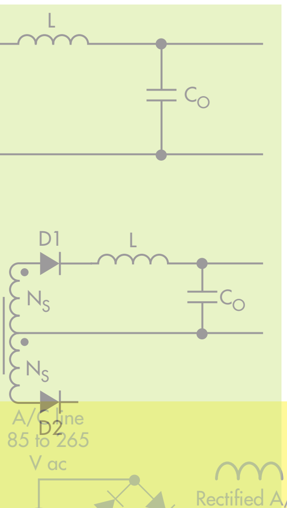
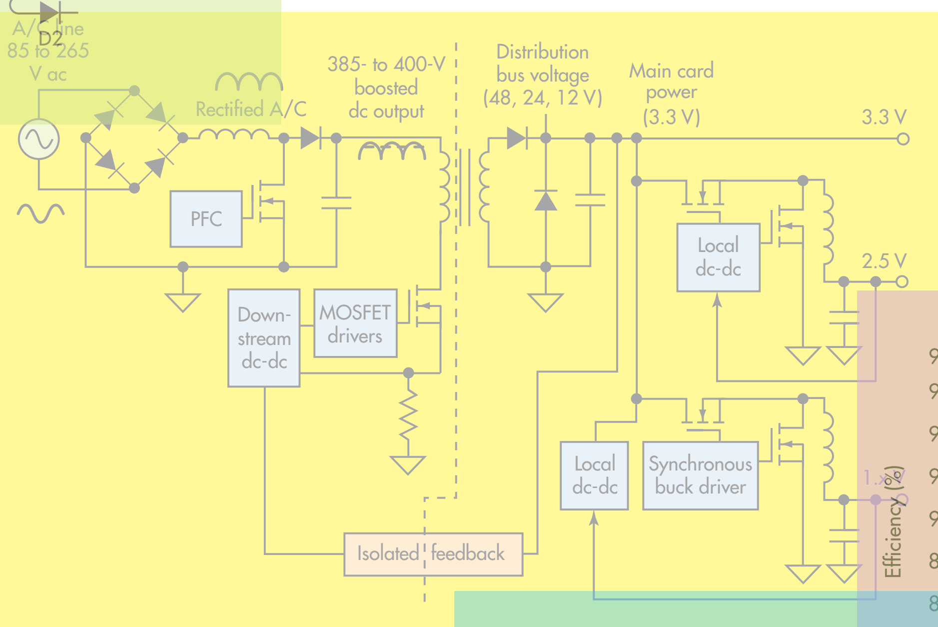
BEST OF GaN Devices





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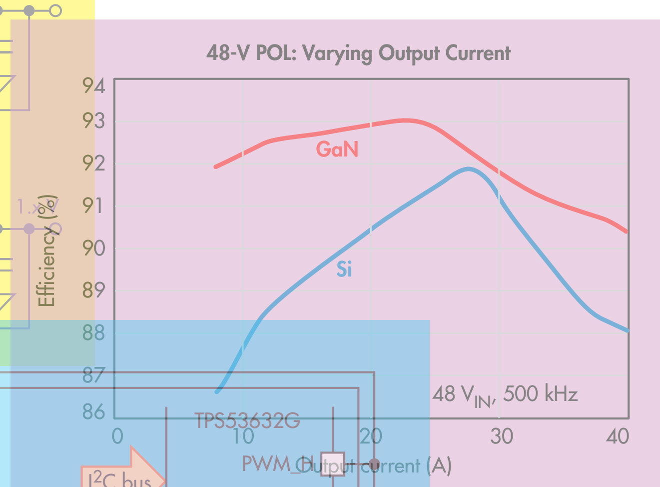

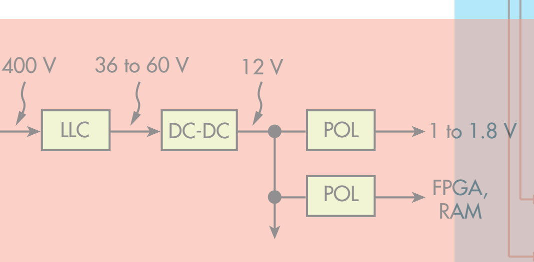

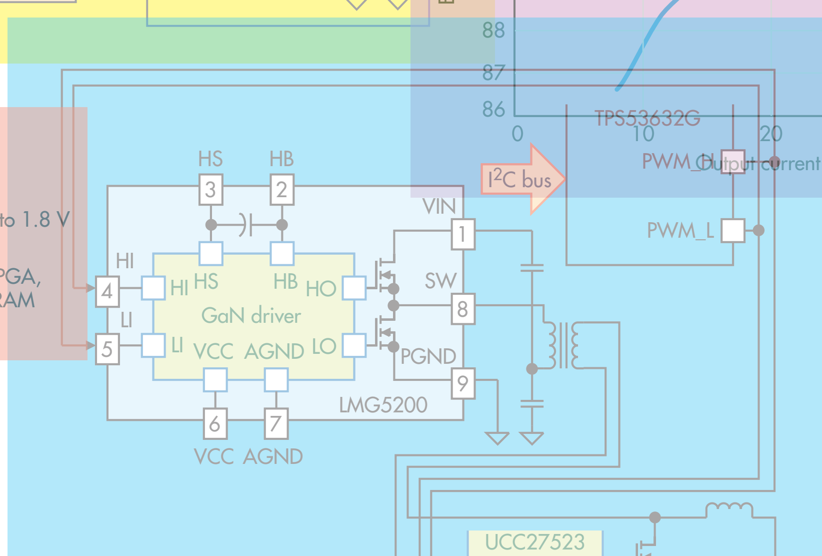

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BEST OF

GaN Devices

INTRODUCTION

Karen Auguston Field,
Content Director

WHILE SILICON MOSFETS have played a dominant role in power supply design in the past, GaN devices are gaining in popularity, due to the fact that they can deliver a smaller footprint, greater efficiency, lower energy consumption, and more. This eBook provides a deep dive into the world of GaN devices and why they are redefining power circuit design today, including an exploration of their many benefits and ways that design engineers can most effectively apply the technology in their designs.

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CHAPTER 1:

GaN FETs Redefine Power-Circuit Designs

LOU FRENZEL, Contributing Editor

The tried-and-true silicon MOSFET has dominated power-supply design, but the tide is turning toward GaN transistors thanks to the latest technology advances.

Silicon MOSFET power transistors have been a mainstay of power-supply design for years. And while they're still widely used, gallium-nitride (GaN) transistors are gradually replacing MOSFETs in some new designs. Recent developments in GaN technology, plus the availability of improved GaN devices and driver circuitry, have more designers looking at the GaN option. GaN offers clear benefits over conventional MOSFETs such as greater switching speeds and higher efficiency.

GaN Devices

GaN power transistors have been around for several years now. Early devices were made on expensive substrates, such as sapphire or silicon carbide (SiC). The primary application was RF power amplifiers for high frequencies. Thanks to their high electron mobility and high voltage tolerance, these devices can generate hundreds of watts of power at frequencies well into the gigahertz range.

Such transistors are called high electron mobility transistors (HEMTs) or pseudomorphic HEMT (pHEMT). HEMTs are a form of metal-semiconductor junction FET using different materials for the gate and channel. These are "depletion-mode" types of FETs, meaning they're naturally "on," unlike the enhancement-mode naturally "off" MOSFETs. HEMT FETs require critical bias networks for proper operation.

A more recent development is the enhancement-mode GaN FET, or eGaN. It's of the insulated-gate variety. Like all GaN devices, they offer the benefits of higher-speed switching, higher voltage operation, and improved heat dissipation. Though enhancement-mode GaN devices are still more expensive than silicon MOSFETs, they're more suitable for power-supply designs and offer a design path to greatly improved performance and efficiency.

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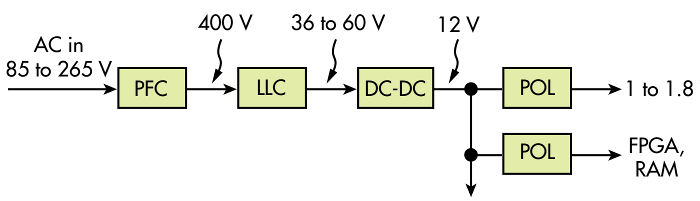
The Case for High-Voltage Designs

Switch-mode power-supply (SMPS) designs are the answer to improving efficiency and conserving energy. Most new designs apply SMPS technology, including regulators, dc-dc converters, point-of-load (POL) converters, and inverters. However, even SMPS designs can be improved.

It has been shown that efficiency declines with each power-conversion stage in the design. Converting high line voltages to low dc supplies for processors and FPGAs typically requires multiple stages of dc-dc conversion and regulation. Reducing the number of conversions is possible if high-voltage devices are available to make the conversion. GaN devices offer that potential.

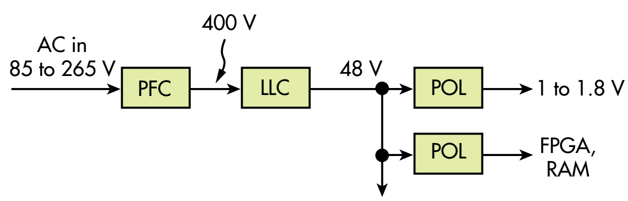
An example is a data-center power system. Data centers contain many high-power servers that require low voltages at high currents. The power is expensive, but so is the cooling that's required. Any savings in the power-conversion path is worthwhile. *Figure 1* shows a typical supply with 120- or 240-V ac input.



1. This power-system configuration is commonly employed in data centers.

A power-factor-correction (PFC) stage is required by the electric utility. This is usually a boost converter with a dc output of 380 V. It's passed to an inductor-inductor-capacitor (LLC) stage that provides a dc output of 36 to 60 V. This is further stepped down by a dc-dc converter, then on to POL converters that provide 1 to 1.8 V dc for the processor, memory, and FPGAs. Each stage takes its toll on efficiency.

Figure 2 shows the solution to this problem. The PFC stage topology is changed with GaN devces that can operate at higher voltages and at higher speeds. The higher switching frequency means that any magnetic devices can be much smaller and more efficient. The LLC stage, also using GaN, downconverts to a 36- to 60-V output utilizing switching frequencies above 1 MHz. A typical output is 48 V to the POL converters, which are exploiting GaN as well. The overall design is not only smaller, but also more efficient.



2. Here, the power system was improved by implementing different circuit topologies and fewer stages to improve efficiency.

Another application involves solar inverters. The solar panel usually drives a dc-dc boost converter. That converter, in turn, operates the dc-ac inverter that provides the 120/240-V ac 60 Hz that ties to the load and the grid. Some systems may include battery storage. Using GaN in both stages and a switching frequency well in excess of 100 kHz greatly improves efficiency over current designs.

In addition to dc-dc converters, POL converters, and inverters, other GaN applications include motor drives and Class D high-power audio amplifiers.

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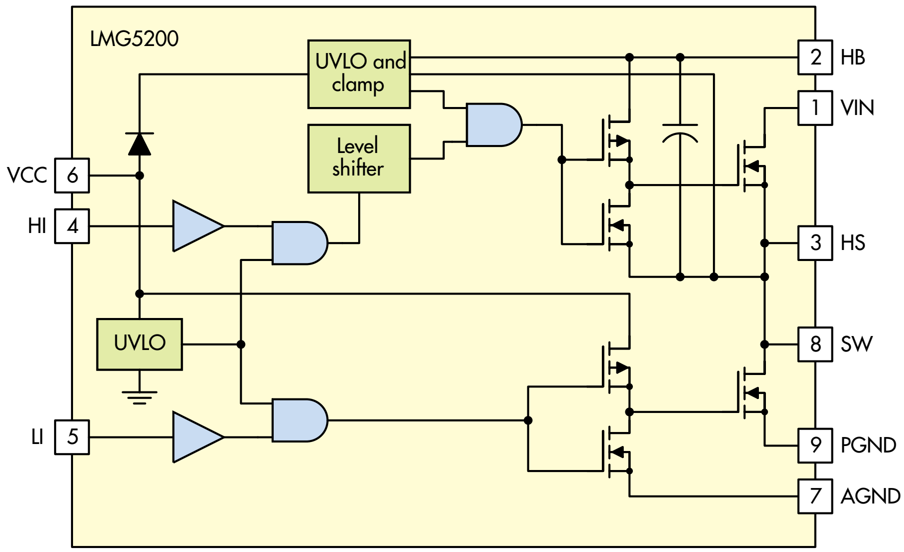

3. The LMG5200 hybrid multichip module, which features two GaN FETs, helps protect against overvoltage and undervoltage.

A Breakthrough Product

Designing with the eGaN FET devices can be challenging mainly due to the tricky gate-drive circuits. In addition to providing the right gate-drive voltage to the GaN power FETs, the circuitry must also provide protection for overvoltage drive or undervoltage conditions.

One device that solves the problem is Texas Instruments' LMG5200. This hybrid multichip module (MCM) contains two 80-V, 10-A GaN FETs in a half-bridge configuration with integral driver. *Figure 3* shows the functional block diagram. Note the undervoltage-lockout (UVLO) protection that prevents the FETs from partially turning on if the input supply voltage falls too low. A clamp also prevents the high-side gate drive from exceeding the FETs' maximum gate voltage.

Features of the LMG5200 include 15-mΩ on-resistance GaN FETs, 80-V continuous or 100-V pulsed rating, gate driver capable of up to 10-MHz switching, TTL inputs, 10-ns minimum PWM width, and 29.5-ns propagation delay. The device comes in a 6- × 8- × 2-mm, 9-lead QFN package. When used with TI's TPS53632G controller, the LMG5200 enables direct conversion from 48 V to 0.5-1.8 V in POLs. An evaluation module is available.

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Thermal considerations for designing a GaN power stage.

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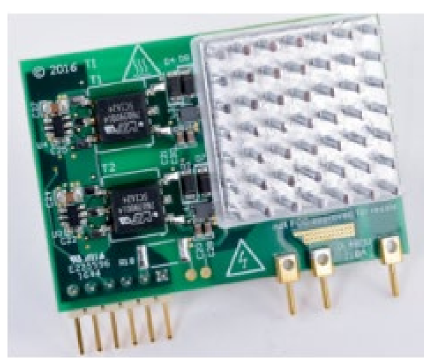
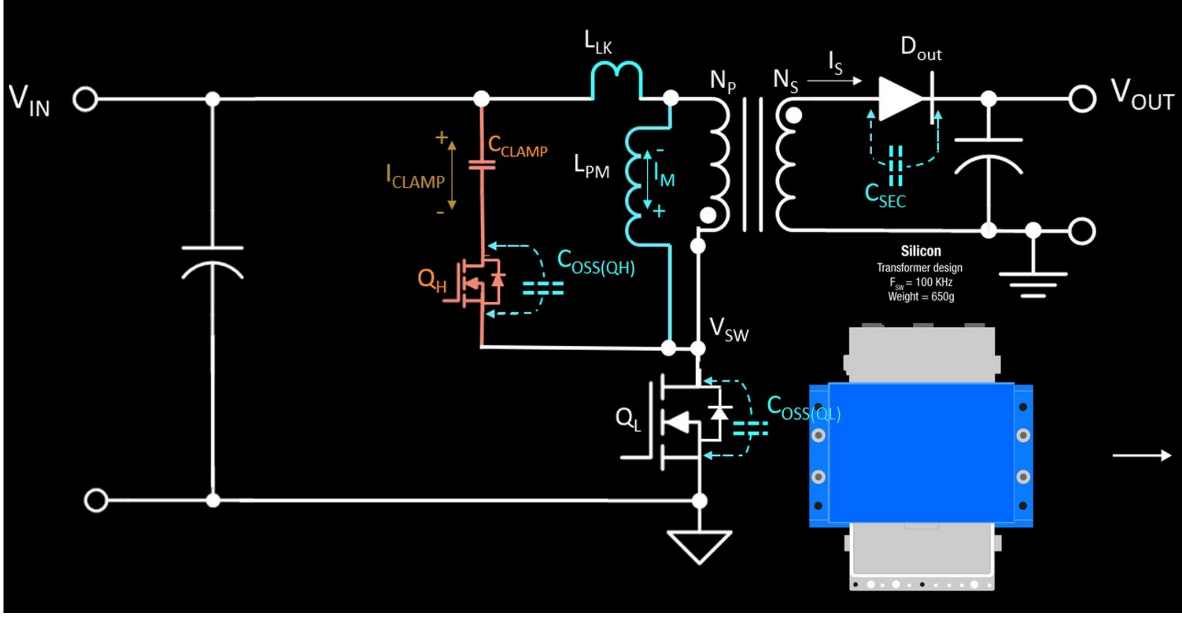




CHAPTER 2:

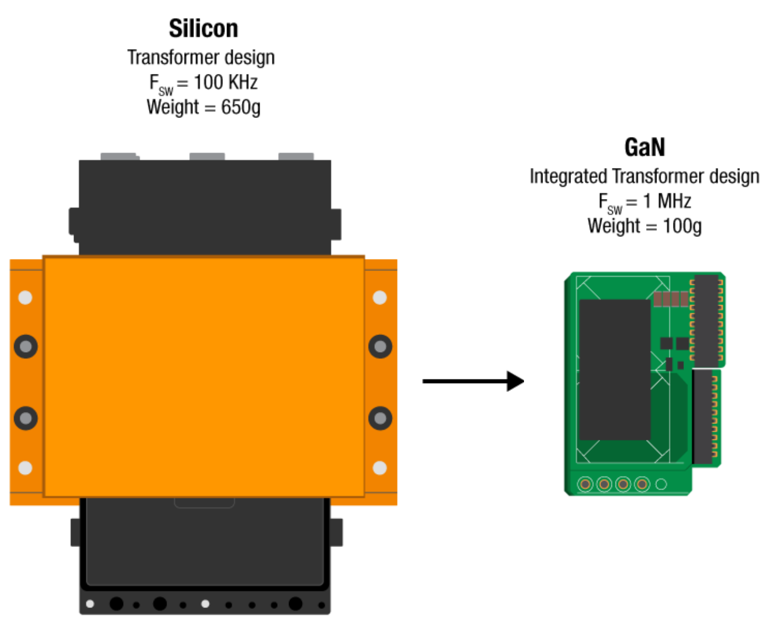
GaN Power Transistors: Master Strokes on a Power-Supply Canvas

PAUL PICKERING, Contributing Editor

Adding gallium-nitride devices such as FETs to power-supply topologies such as the active-clamp flyback can lead to a variety of performance improvements.

It's not news that the efficiency of switching power supplies is now above 90% in many applications. At those levels, it becomes progressively harder to eke out small improvements.

The introduction of power devices made from wide-bandgap (WBG) semiconductors such as gallium nitride (GaN) and silicon carbide (SiC), instead of silicon, has given designers some important new tools *(Fig. 1)*.



1. Changing from silicon to GaN in a power supply can slash the size of magnetic components such as transformers.

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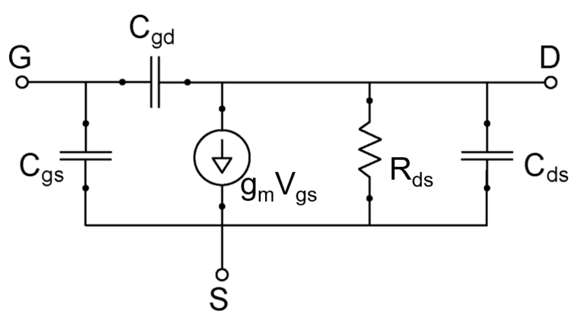
Material	Silicon	GaN	SiC	Impact
Bandgap (Eg), eV	1.1	3.4	3.26	Lower leakage, higher operating temperature
Breakdown field (Vbr), V/μm	30	300	200 - <300	Higher breakdown voltage for the same die
Electron mobility (μe), cm²/V·s	1,500	1,500	700	On par
Thermal conductivity, W/cmK	1.3	>1.5	<3.8	More efficient cooling, higher operating temperature
Dielectric constant, μr	11.7	9	9.7	On par

2. Wide bandgap semiconductors such as GaN and SiC offer superior performance over silicon in power applications.

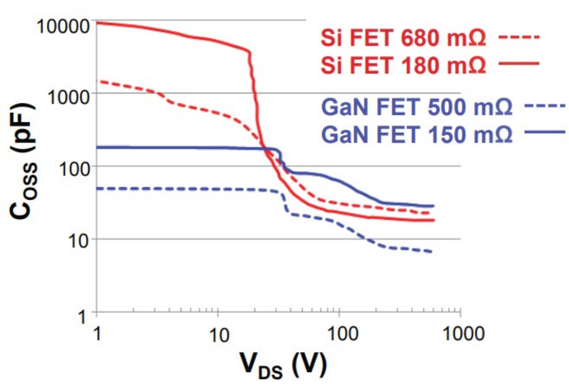
In a power supply, changing from silicon MOSFETs to transistors based on gallium nitride (GaN) yields efficiency improvements. A GaN device *(Fig. 2)* has lower on-resistance $R_{DS(ON)}$ than a silicon device. It also has a higher breakdown voltage, can operate at higher temperatures, and has far superior reverse-recovery characteristics. The GaN device also incurs much lower switching losses, so it can operate at higher switching frequencies. As shown in Fig. 1, this can lead to a dramatic reduction in the size of the design.

Higher switching frequencies reduce power converter size, weight, and cost because they allow the use of smaller capacitors, inductors, and transformers. Switching to GaN power devices can cut the size of a power supply by up to 50%.

Let's examine in more detail the advantages of switching to GaN, beginning by reviewing the simplified high-frequency model of a power MOSFET in *Figure 3*. This model applies to both silicon and GaN technologies.



3. A simplified high-frequency equivalent circuit of a MOSFET.



4. Variation of COSS with VDS and RDS(ON) for GaN and Si FETs.

It includes parasitic junction capacitances C_{GD}, C_{GS}, and C_{DS}. In the datasheet, these are stated as the input capacitance (C_{ISS}), the output capacitance (C_{OSS}), and the reverse transfer capacitance (C_{RSS}), where:

$C_{RSS} = C_{GD}$

$C_{ISS} = C_{GS} + C_{GD}$

$C_{OSS} = C_{DS} + C_{GD}$

The parasitic junction capacitances are formed from a series combination of a bias-independent oxide capacitance and a bias-dependent depletion capacitance. C_{OSS} decreases for lower values of $R_{DS(ON)}$. For a given device, C_{OSS} is also nonlinear and decreases significantly above a V_{DS} threshold.

The shape of the curve is significantly different for Si and GaN devices. As shown in *Figure 4*, for a GaN FET, C_{OSS} is proportional to $R_{DS(ON)}$ and varies very little for V_{DS} < 30 V.

For a silicon FET, on the other hand, C_{OSS} steadily increases as V_{DS}

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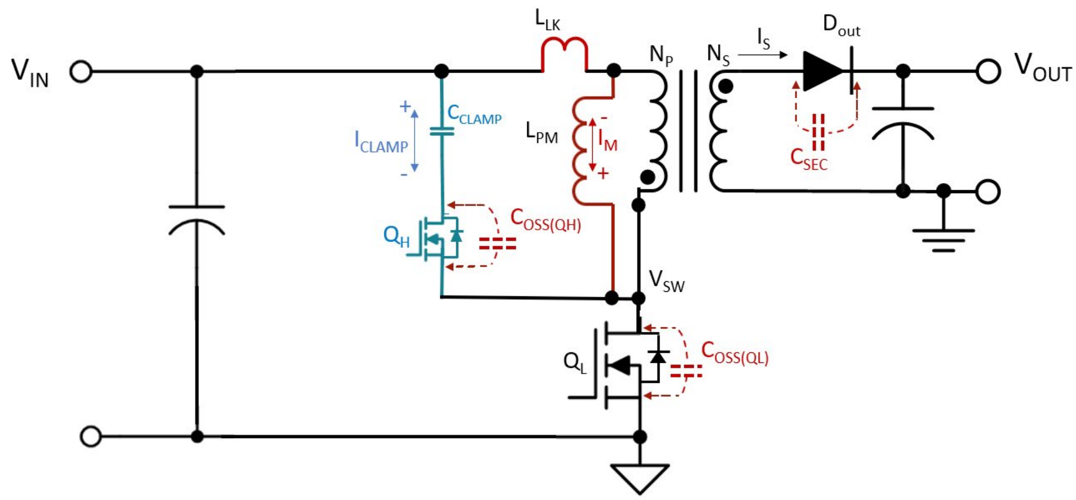

5. The active-clamp flyback converter, showing the MOSFET body diodes and some of the equivalent circuits.

decreases below 30 V, but the increase isn't proportional to $R_{DS(ON)}$. For the device in Figure 4 with $R_{DS(ON)}$ = 680 mΩ, C_{OSS} at V_{DS} = 30 V is about 100X larger than its value at V_{DS} = 400 V. For another device with $R_{DS(ON)}$ = 180 mΩ, C_{OSS} is almost 300X larger over the same V_{DS} range.

A silicon MOSFET also has a body diode—it's an intrinsic PN junction formed during the manufacturing process. One consequence of the body diode is an undesired reverse-recovery charge when the diode turns off. GaN FETs don't have an intrinsic body diode, so there's zero reverse-recovery charge.

Application Example: The Active Flyback Converter

As we can see, the characteristics of Si and GaN devices are significantly different, but how does changing from silicon to GaN improve performance in a power supply? Let's use the active-clamp flyback (ACF) converter as an example. The ACF is a popular choice for small power adapters because it combines high power density with high efficiency.

Figure 5 shows the ACF circuit. The active clamp consists of a high-side secondary switch (Q_H) in series with a clamp capacitor (C_{CLAMP}). This circuit uses silicon devices, hence the body diodes.

Also shown in Fig. 5 are some essential equivalent circuit elements: the output capacitances (C_{OSS}) for Q_H and Q_L; and the secondary rectifier capacitance (C_{SEC}). The transformer can be modeled as a transformer leakage inductance (L_{LK}) in series with a primary-side magnetizing inductance (L_{PM}).

The purpose of the active clamp is to recycle the energy stored in the transformer leakage by storing it in C_{CLAMP}. The circuit then delivers the energy to the output later in the switching cycle to minimize the voltage spike at the transformer primary side, thus reducing the voltage stress on the main switch Q_L.

Controlling the timing of the active clamp switch can also eliminate switching loss by turning on Q_L at the zero-volt switching point (ZVS operation). ZVS operation allows the ACF switching frequency to be higher, reducing the size of the power supply.

Figure 6 shows the switching events in the ACF sequence, beginning with primary

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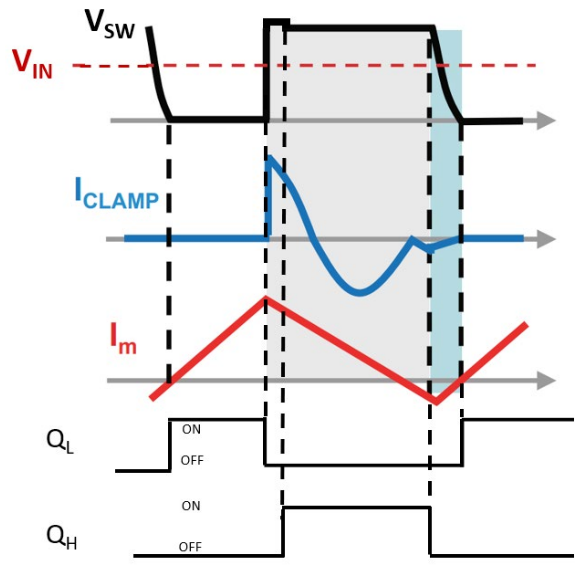

6. The principal currents and voltages of the ACF during a ZVS switching cycle.

power switch Q_L and clamp switch Q_H both off. Note that both I_{CLAMP} and I_M are bidirectional as shown in Fig. 5 above: the direction is denoted in the discussion by, for example, $I_{M(+)}$ and $I_{M(-)}$.

A summary of the active-clamp ZVS operation follows. Consult this paper for an in-depth discussion.

1. Q_L turns on: $I_{M(+)}$ is linearly increasing, storing energy in the primary-side magnetizing inductance L_{PM}.
2. Q_L turns off: $I_{M(+)}$ charges the junction capacitance of Q_L ($C_{OSS(QL)}$) and discharges both the junction capacitance of Q_H, ($C_{OSS(QH)}$) and the junction capacitance of the secondary rectifier (C_{SEC}). Therefore, the current on Q_L (I_{QL}) decreases, the clamp current (I_{CLAMP}) increases, and the secondary rectifier current (I_S) increases with V_{SW} rising from 0 V to a high level. $I_{M(+)}$ flows through the body diode of Q_H to charge C_{CLAMP}.
3. Q_H turns on: Q_H is conducting, NVOUT starts to demagnetize L_{PM}, so $I_{M(+)}$ starts to decay, and L_{PM} releases its energy to the output. At the same time, C_{CLAMP} absorbs the L_{LK} energy by resonating with L_{LK}; therefore, I_{CLAMP} is in the positive direction.
4. Q_H turns off: The negative magnetizing current, $I_{M(-)}$, starts to discharge $C_{OSS(QL)}$, charge $C_{OSS(QH)}$, and charge the C_{SEC}, so V_{SW} decays to 0 V.
5. The sequence then repeats: Q_L turns on as V_{SW} reaches 0 V, giving ZVS operation.

For ZVS to occur, the energy stored by L_{PM} with current $I_{M(-)}$ must be greater than or equal to the energy stored in the lumped capacitance (C_{SW}):

$$\frac{1}{2}L_{PM}{I_{(M-)}}^2 \geq \frac{1}{2}C_{SW}{V_{SW}}^2$$

The equation also shows that a larger C_{SW} requires higher $I_{M(-)}$ for ZVS.

The ACF topology achieves higher overall efficiency than other flyback designs. *Figure 7* depicts a qualitative comparison. The ACF's clamp and switching losses are virtually zero, but improvements can still be made in other areas.

Building up the additional negative current increases the flux density. Thus, the ACF core loss is slightly higher than that of a flyback design with a passive clamp. In addition, the ACF clamp current flows in the transformer primary winding during demagnetization time, increasing the winding loss. if the transformer losses become too large, they can negate the efficiency gains of the ACF.

Switching to GaN Reduces ACF Power Losses for Increased Efficiency

Changing to a GaN FET reduces these losses. GaN's lower C_{OSS} results in lower peak-to-peak I_M. A lower I_M, in turn, leads to lower core loss; lower primary current for less

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Topology	P_{CLAMP}	$P_{SWITCHING}$	P_{CORE}	$P_{WINDING}$
A: passive clamp/DCM	High	High	Higher	Mid
B: passive clamp/TM	High	Mid	Lower	Lower
C: active clamp/TM	≈0 (to output)	≈0 (ZVS)	Mid	Higher

7. A comparison of the relative losses in three flyback converter designs.

winding loss; and lower clamp current for less conduction loss in Q_H.

Figure 8 compares the primary-current and clamp-current waveforms of two ACFs with Si and GaN FETs, respectively. Each FET has a similar $R_{DS(ON)}$, and each circuit uses a Schottky diode as the secondary rectifier. The GaN device gives a reduction of more than 22% in peak-to-peak I_M and RMS primary current I_{PRI} compared to a Si FET.

GaN Improves ACF Efficiency at Light Loads

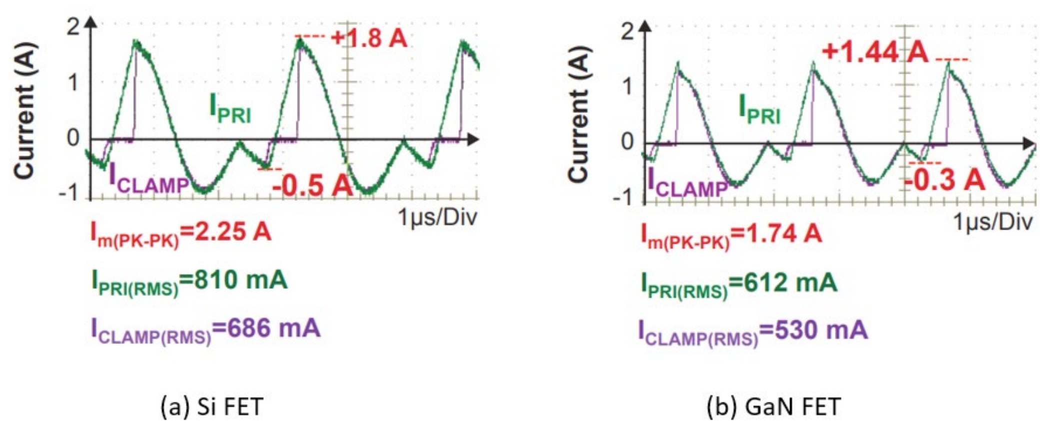
It's not only the difference in magnitude of C_{OSS} between Si and GaN that affects the ACF performance. The nonlinearity difference has an effect, too, particularly in the efficiency of the ACF under light loads.

As the load current becomes lighter, the current-mode control loop reduces the positive peak current $I_{M(+)}$ to regulate the output power, while the negative magnetizing current $I_{M(-)}$ doesn't change, assuming a constant input voltage. $I_{M(+)}$ delivers energy to the output, while $I_{M(-)}$ stores the circulating energy for ZVS operation.

If $I_{M(+)}$ and $I_{M(-)}$ become closer in magnitude as the load decreases, the transformer's efficiency drops, and the losses increase since the contribution of the circulating energy is greater.

A silicon-based ACF with its highly-nonlinear C_{OSS} has a larger $I_{M(-)}$, especially at high input voltage $V_{BULK.}$ At light load, the impact becomes more significant, and the efficiency deteriorates very quickly. The measurement result in *Figure 9* shows that the efficiency difference between 50% load and 25% can be as high as 7.3%.

In comparison, a GaN's lower C_{OSS} results in a relatively lower $I_{M(-)}$. Its impact is smaller



8. A comparison of current waveforms highlights GaN's superior ACF performance.

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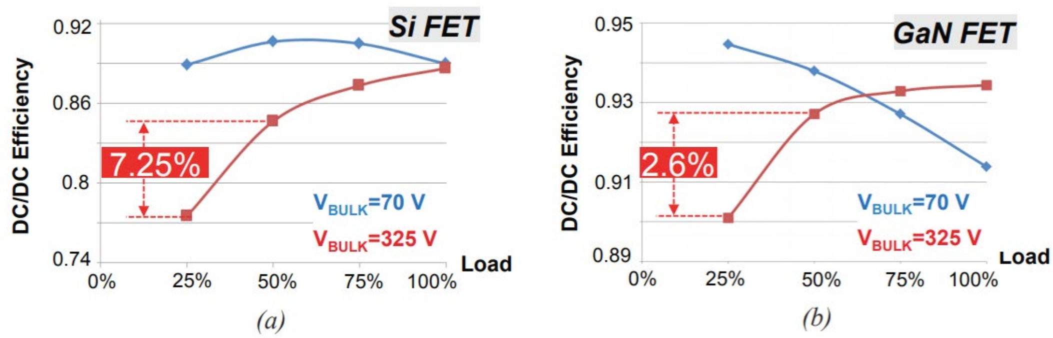


9. The efficiency of an ACF with a silicon FET degrades more under light loads than a GaN-based design.

under light loads, though, with only a 2.6% difference in efficiency between 50% load and 25% load.

Driving the GaN: The Other Piece of the Puzzle

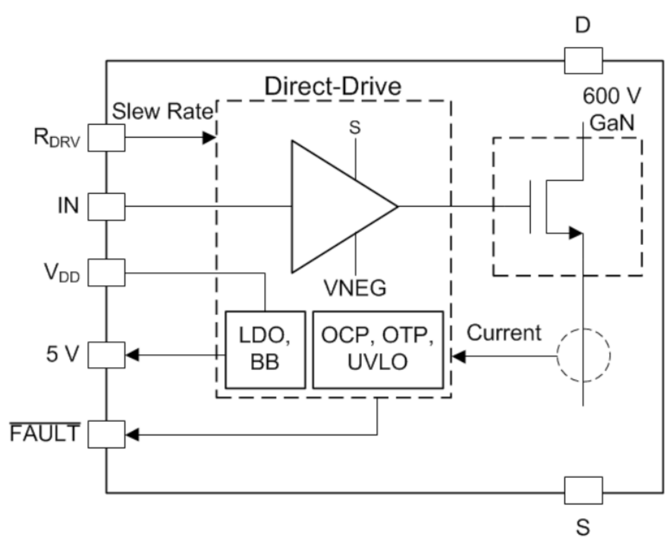
The GaN transistor provides significant performance improvements to the ACF and other power designs, but it presents challenges for the driver circuit. Designers can't just swap in a GaN device for its Si counterpart. For one thing, traditional GaN FETs are depletion-mode (normally-on), whereas Si MOSFETs are normally-off enhancement-mode devices.

To provide drop-in replacements for Si MOSFETs, GaN FET switch suppliers must use another switch in series to provide the required normally-off functionality. A typical solution pairs a depletion-mode GaN with a silicon driver in a cascode configuration.

An alternative approach is to redesign the device as normally-off enhancement mode. Enhancement-mode devices have other issues, such as different driver requirements than an equivalent silicon device. For example, the maximum allowable V_{GS} for an enhanced GaN FET is 6 V—lower than for silicon.

For both types, the higher switching frequency of a GaN transistor demands greater timing precision in the switch-driving signal. GaN switches are also highly sensitive to parasitic impedances from packages, interconnects, and outside sources.

Manufacturers offer both general-purpose GaN drivers and integrated solutions for defined applications. TI's UCC28780, for example, is an ACF controller with ZVS capability that offers switchable GaN or Si drive circuits. The ZVS portion incorporates auto-tuning, adaptive dead-time optimization, a variable



10. The LMG341xR070 combines a 600-V GaN FET with a driver and protection circuitry.

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switching-frequency control law, and adaptive multimode control that changes operation based on input and output conditions. These features allow the UCC28780 to achieve ZVS over a wide operating range.

Integrating a GaN FET, a driver, and protection circuitry into a single package is another option. The LMG341xR070 *(Fig. 10)* provides an alternative to cascode GaNs or standalone devices with separate drivers. The device's gate driver enables 100-V/ns switching with near-zero V_{DS} ringing; current-limiting circuitry protects against unintended shoot-through events. Overtemperature shutdown prevents thermal runaway, and system interface signals provide self-monitoring capability.

Resources

Texas Instruments has multiple resources to help engineers add GaN devices in their designs. The GaN overview page is a good place to start; it contains GaN-related white papers, application notes, product pages, and reference designs.

We discussed the operation of the ACF in this April 2018 article. Pei-Hsin Liu's paper at the 2018 Texas Instruments Power Supply Design Seminar also reviews ACF operation in great detail. The seminar includes a set of training videos on the same topics, too. For another example of GaN-related improvements, consult this series of videos on resonant converter topologies.

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Optimized gate drive layout offers high reliability with over-current protection.

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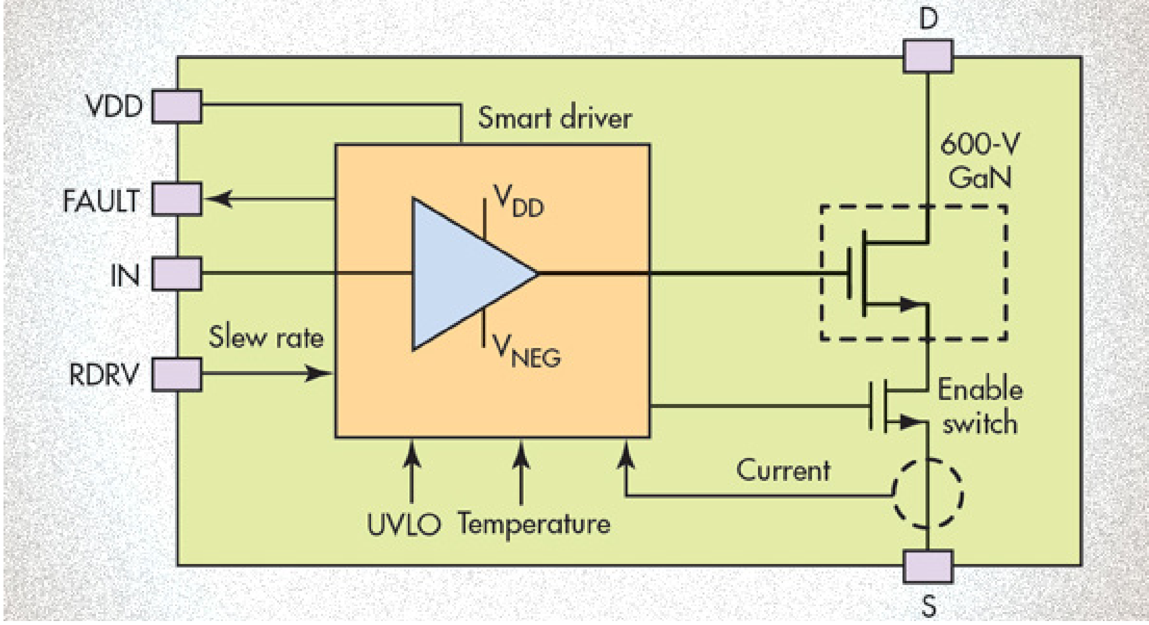

CHAPTER 3:

High Voltage and GaN: Gateways to Better Power-Supply Efficiency

LOU FRENZEL, Contributing Editor

Lower resistance and faster switching leads to less heat and lower energy consumption.

Every electronic device has a power supply. Most of those power supplies are of the switch-mode variety, which offer good efficiency. These include ac-dc supplies, dc-dc converters, ac motor drives, and inverters for solar-power conversion. Yet, as recent developments show, efficiency can be further improved by using GaN semiconductor devices and high-voltage techniques. These and other benefits can be realized thanks to the arrival of new products.

The Problem

Switching power supplies have brought greater power efficiency to electronic products. In an era of ever-increasing electronic product usage, efficiency has become a primary design objective, be it for portable battery-powered items or mains-powered commercial and consumer equipment. It's also a top priority in industrial equipment designs.

There's no better example of the need for greater efficiency than data centers. With thousands of servers routing internet connections, a data center burns more electricity than almost any other commercial facility. And that doesn't include the massive cost of air conditioning to keep all of those servers cool. Even small improvements in efficiency can greatly reduce electrical and cooling costs.

The losses that most contribute to inefficiency include the on-resistance and turn-on/turn-off time of switching devices. Most switching supplies use standard silicon MOSFETs. The devices consume no power when off, of course. When switched on into a saturated state, they do burn some power because of their conduction resistance, low as it may be.

Another factor is switching time. As the MOSFET switches from on to off and vice versa, the device passes through its linear region, where it consumes power. The slower the rise and fall times, the more power burned.

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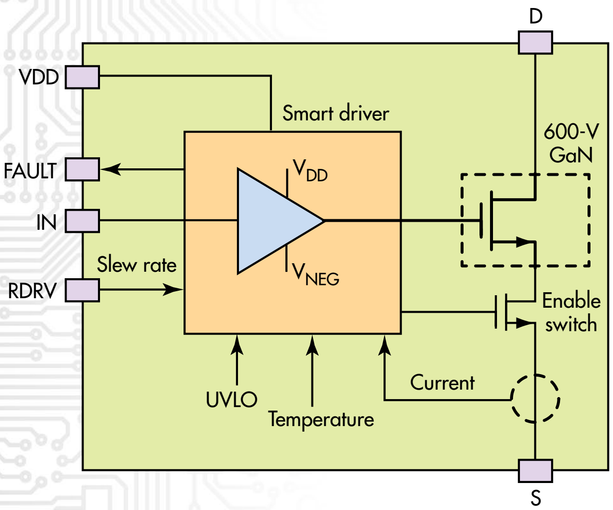

Texas Instruments' LMG3410 is single-stage GaN power MOSFET with an internal smart driver that simplifies design while delivering the benefits of high frequency, high voltage, and low on-resistance.

The obvious solution is to find a faster device with lower on-resistance, if it exists. And oh by the way, make sure the device can handle the high voltages usually encountered in commercial- and industrial-grade equipment.

Finally, the design architecture of the power supply should be reconsidered. Especially important is the number of energy-conversion stages used in the design. Each stage introduces its own inefficiency, compounding the problem.

The Solution

As a first step in design, minimize the number of energy-conversion stages. Each stage of rectification, regulation, dc-dc conversion, or other energy-transfer process adds a level of inefficiency. One approach to this is to start with higher voltages and use fewer stages. Higher voltage usually means less current. Higher-current, low-voltage circuits always consume more power.

Keep in mind the basic premise behind the electric utility's reason for long-distance transmission of electrical power at kilovolt levels. Higher voltages result in lower current for a given power, which produces less voltage drop per mile of transmission line.

The goal is to start with higher input voltages, ac or dc, and bring them into the supply and convert to lower voltages as quickly as possible. Use the 480- or 240-V ac lines or the solar-array dc output of hundreds of volts directly. Electric car chargers use 240 V ac and the car batteries are usually several hundred volts. The secret to a high-voltage design is to find the HV components like diodes and transistors that can handle this voltage.

High-voltage diodes have been available for years and standard silicon MOSFETs continue to improve. They can handle voltages up to about 1000 V with reasonably fast switching and low on-resistance. However, one newer device with the greatest potential in power supplies is the GaN MOSFET. These gallium and nitrogen compound devices naturally switch faster and have lower on-resistance than their silicon counterparts. Moreover, they can handle the HV.

GaN devices have met with big success as microwave and millimeter-wave RF power amplifiers. These high-voltage devices provide hundreds and even thousands of watts of power at ever-increasing radio frequencies. Now GaN devices are being optimized for power-conversion applications.

One benefit of adopting GaN devices is that the power supply can be switched at higher frequencies beyond the usual several hundred kilohertz. Using switching rates above 1 MHz allows ripple to be reduced using smaller capacitors and inductors. Filtering becomes easier, and the smaller components make it possible to shrink overall size.

One key issue with GaN devices is that they are depletion-mode MOSFETs—they normally conduct and thus have to be driven off with a gate input. Standard silicon MOSFETs are enhancement-mode devices that are normally off and must be gate-driven to turn them on. Such devices are easier to use and drive circuits are simpler.

GaN MOSFETs, on the other hand, require special, more-complex drive circuits. This is an issue worth dealing with as switching times are faster in the nanosecond region. In addition, on-resistance drops down into the tens of milliohms range.

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An Example Solution

Newer silicon MOSFETs do provide some improvements in efficiency. However, even better alternative solutions for switch-mode power designs are now available. One of these is a silicon-carbide (SiC) MOSFET that provides not only lower on-resistance and faster switching, but also very high voltage tolerance. An even better choice, though, is a GaN device with improved specifications. An example is Texas Instruments LMG3410 GaN power device (see figure).

It's a single GaN MOSFET with internal driver circuits that simplifies design and application. It can handle up to 600 V and 12 A. The device is usable in designs with up to 1-MHz steady-state operation. Propagation delay is 20 ns, and switching time is adjustable over the range of 25 to 100 V/ns, making it possible to control EMI while optimizing efficiency. On-resistance is a low 70 mΩ.

Looking at the figure, a key feature of the LMG3410 is its internal gate driver that keeps the GaN transistor off in its normal state. An internal dc-dc converter generates the negative voltage needed to keep the device biased off. An input signal in the 3- to 5-V range turns the GaN device on. When the device is unpowered, a series silicon MOSFET keeps the GaN device disconnected or off.

The LMG3410 also has multiple safety and protection features that include undervoltage lockout (UVLO) as well as overcurrent and overtemperature protection. A fault output signal indicates the device's status. All of this is housed in an 8- × 8-mm QFN package.

When designing a new switch-mode supply, take a look at some of the newer devices like those mentioned. Even single-digit improvements in efficiency can go a long way toward reducing power consumption and heat. Furthermore, operating at higher frequencies enables the use of smaller capacitors, inductors, and other components, resulting in more compact packages that are easier to cool. Cost reductions are possible.

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GaN drives energy efficiency to the next level.

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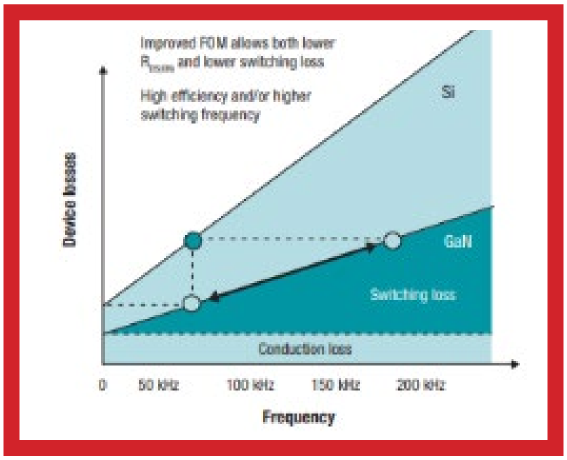

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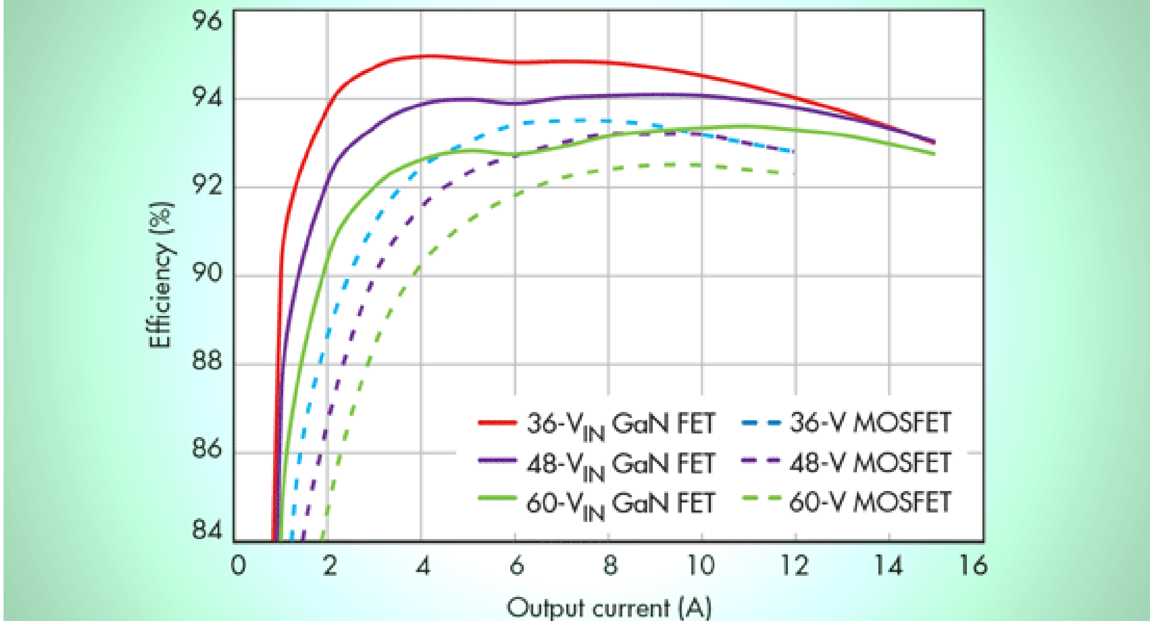

CHAPTER 4:

Thoughtful Board Design Unlocks the Promise of GaN

Penton Freelance Staff

Texas Instruments Gallium-nitride (GaN) transistors fabricated on silicon substrates can boost efficiencies and help shrink the footprint of power supplies.

Power transistors with faster switching speeds will enable power supplies with smaller form factors and higher energy transfer efficiencies. Indeed, the elimination of heat sinks will give designers the ability to visualize entirely new form factors for power bricks and modules, including those enabling wireless power transfers. Companies like Texas Instruments and Efficient Power Conversion (EPC) are focusing on applications requiring compact form factors and high energy-transfer efficiencies.

Incorporation of gallium-nitride (GaN) transistors, fabricated on inexpensive silicon substrates, represents an improvement over conventional silicon MOSFETs. The faster switching speed and lower on-resistance of GaN devices makes possible smaller devices with lower heat dissipation. Low-voltage transistors in chip-scale packaging have footprints as small as 0.9 × 0.9 mm. Thus, with thoughtful board and package design, low-voltage GaN devices can shrink the size of power bricks and modules.

However, the substitution of GaN transistors for MOSFETs is not one-to-one. The layout must minimize the inductive path between the power-stage devices and their drivers to avoid impairing performance. And gate-drive requirements will vary from one GaN device to another; low-voltage devices can be sensitive to overdrive.

Board layouts for GaN transistors must account for parasitics, which are less prominent in slower MOSFET systems. Particularly, designers must minimize the inductive path between the source of the driver and the FET transistor's gate. Without that, says TI's Systems Architect Michael Seeman, it's like installing a 500-hp engine under the hood of an economy car. Without a matching frame transmission, and suspension, you can do serious damage.

As a result, engineers using GaN must isolate the source-to-gate-drive path from any common-mode inductances. (EPC's transistors fortunately use a low-inductance package

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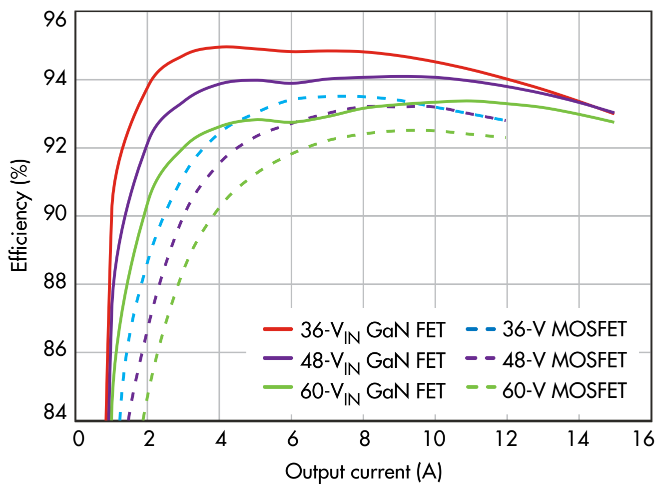

1. The graph displays GaN FET efficiency versus a traditional MOSFET.

with solder bar interconnects.) The avoidance of overdrive is another serious engineering issue: EPC's eGaN FETs can be damaged by gate drive greater than 6 V. Consequently, some FET drivers (like TI's LM5113) will hold the GaN FET drive to 5.25 V with an internal clamping circuit.

Improved POL Efficiency: Low-Hanging Fruit

The existing literature (pairing the LM5113 gate driver, for example, with EPC2001 eGaN FETs) compares the design of a dc-dc power converter using 36-V GaN transistors to a dc-dc with 36-V silicon MOSFETs. By eliminating heat sinks, the brick using GaN FETs is a fraction of the size of the brick using FETs. And a small but significant difference occurs in energy transfer efficiency.

In a 1/8th brick converter dropping a 36- to 75-V input to a fixed 12-V output, the operation of several low-voltage GaN FETs was compared with MOSFETs with the same voltage and current ratings. The efficiency of a 36-V GaN FET was compared with the efficiency of a 36-V MOSFET; the efficiency of a 48-V GaN FET was compared with a 48-V MOSFET, and so on for 60-V systems. Switching speeds for higher-voltage devices under load are a bit slower than lower-voltage devices. But in this demonstration, the devices were clocked similarly: The dc-dc converter with GaN FETs was clocked at 333 kHz, while the circuit with MOSFETs was clocked at a familiar 250 kHz.

Not surprisingly, the dc-dc with 36-V GaN FETs showed the highest efficiencies, better than 94% for current loads from 2A to 12A (better than 92% out to 15 A) (see "Gate Drivers for Enhancement Mode GaN Power FETs"). Among the 60-V circuits, the GaN FETs offered better than 92% for all loads above 4A, while the MOSFET efficiency reached 92% only above 6A *(Fig. 1).*

In a similar demonstration, the efficiency of a 48- to 12-V switching regulator using TI's LMG5200 driver circuit pushing 80-V GaN FETs was compared with a MOSFET-based dc-dc converter (see "GaN FET Module Performance Advantage over Silicon"). The LMG5200 incorporates a controller/driver and two 80-V FETs in a 6- × 8-mm QFN package. In the efficiency demonstration, it was clocked at 1 MHz.

The MOSFET-based implementations were switched at a conventional 250 kHz and again at 800 kHz. Predictably, the circuit with GaN transistors exhibited fewer switching losses. The 80-V MOSFET at 250 kHz actually delivered better than 92% efficiency under

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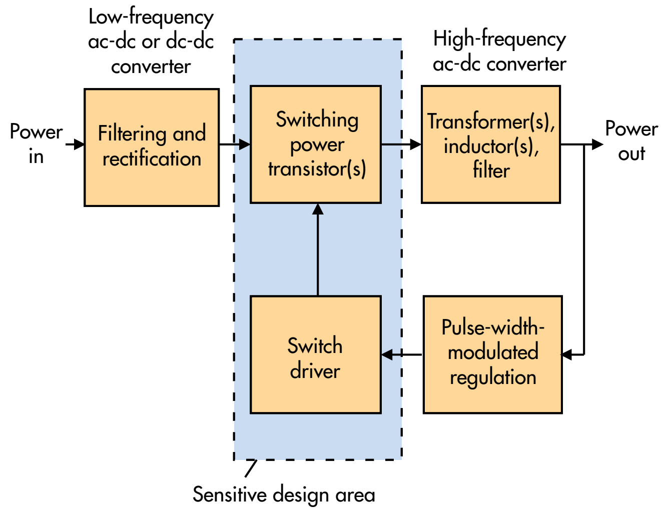

2. Generic functions of a switched-mode power supply include a pulse-width modulator, power stage, and LC network.

a range of current loads out to 6 A. The LMG5200 circuit demonstrated better than 94% efficiency from 4 to 10 A.

In point-of-load (POL) supplies, the difference in efficiencies—even 1% or 2%—can be significant. In a telecomm switching station, for example, where a 48-V intermediate voltage must be dropped to 12 V or less on literally thousands of POL supplies, the savings in electrical energy can amount to thousands of dollars per year. For dc-dc converters, consequently, GaN is an enabling technology.

The Anatomy of a Switching Regulator

In operation, a dc-dc converter is essentially a power pump, based on a sawtooth oscillator, drumming out pulses at a predictable cadence. (The voltage and currents applied to the load are governed by the width and frequency of the pulses.) Three essential elements make up the chain *(Fig. 2):*

- A pulse-width modulator (PWM), and control logic.
- A power stage (typically two power transistors, a high-side and low-side device, and their gate drivers), which pulls current from the power source, and feeds it to the load.
- An LC network to smooth the pulses.

The operation of a switching power supply (overly simplified) can be visualized as a steam shovel moving a mountain of dirt from one location to another. Think how long it takes the shovel to scoop up the dirt in one place and dump it at another. Think how much dirt is left behind. Imagine what the transfer would look like if the steam shovel were replaced by a teaspoon making dirt transfers a million times a second. This is a model for a switching power supply of the future—ever faster and smaller energy transfers.

But switching power pulses under load remains a challenge: The higher the voltages and currents moved, the more sluggish the switching speeds are likely to be. Thus, the sweet spot for switching power-supply design remains doggedly at 250 kHz. There are high-efficiency parts operating at 1-MHz commutation rates, but switching regulators operating at (say) 10 MHz (and small enough to incorporate spiral inductors on-chip) are still a rarity.

GaN's faster switching speeds, despite the attention required for packaging and board layout, are an enabler for power-supply efficiencies. At the very least, it reduces the size and cost of the inductors. Longer term, it allows for a re-invention of the power-manage-

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ment function. GaN devices are considered high electron mobility transistors (HEMTs). The availability of “enhancement-mode devices,” which enable GaN transistors to turn-on/turn-off with the application of positive gate voltages, will encourage MOSFET system builders to experiment.

The TI LMG5200 GaN FET power stage EVM actually serves as an evaluation tool for potential GaN converts. TI says the LMG5200, by itself, offers measurable performance improvements across a wide variety of applications. These applications include multi-megahertz synchronous buck converters, Class D amplifiers for audio, and 48-V POL converters for telecommunications servers.

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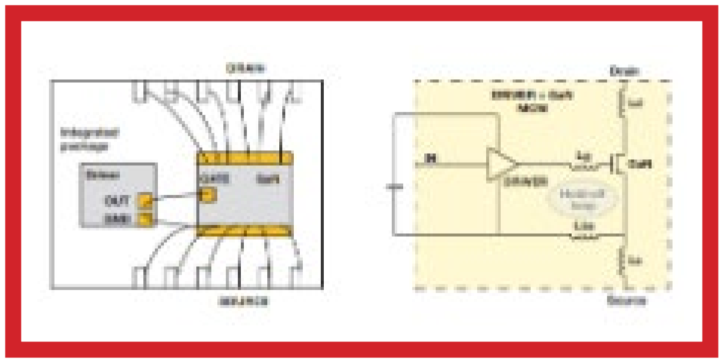

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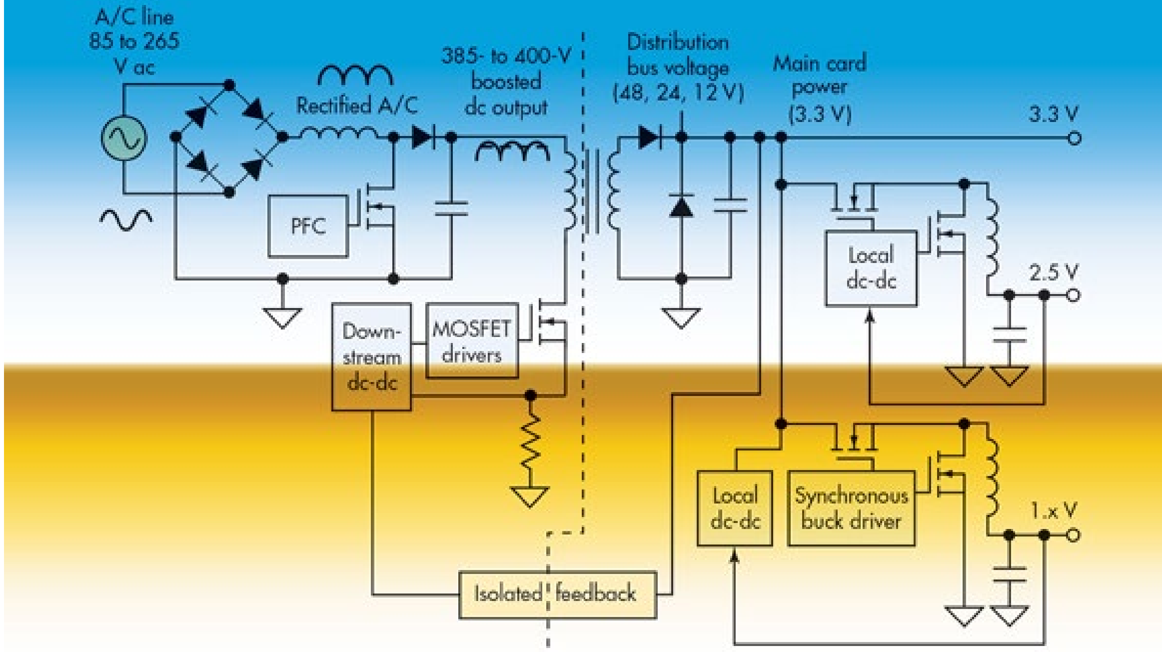


CHAPTER 5:

GaN Devices Bring Benefits to POL DC-DC Converter Designs

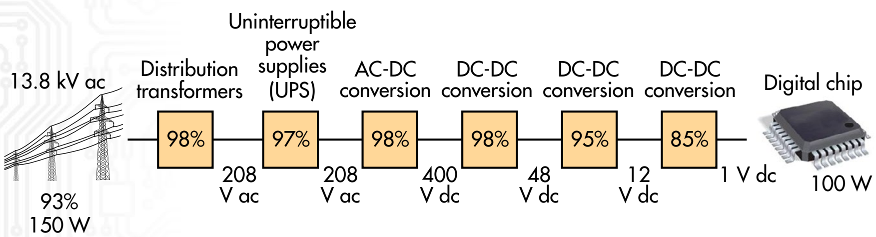
PAUL PICKERING, Contributing Editor

To get the most out of the advantages GaN transistors can offer in low-voltage, high-current POL converter design, pay close attention to several key guidelines.

It comes as no surprise that a large-scale data center, enterprise server, or telecom switching station uses a lot of power. Data-center electricity consumption in the U.S. is projected to increase to roughly 140 billion kilowatt-hours annually by 2020. This usage is equivalent to the output of 50 power plants; the total data-center electricity bill is around $13 billion annually.

Figure 1 shows a typical power-conversion architecture for a data-center server farm. Although most of the stages are extremely efficient, the overall result is an efficiency of only around 67%. The last two dc-dc stages are not only the least efficient, they're also located in the most space-constrained environment: the server rack or motherboard. Since the wasted energy is dissipated as heat, decreased efficiency here leads directly to increased cooling costs. Thus, designers always strive to boost the performance of these stages.

Many designers of such systems are standardizing on a 48-V power-distribution architecture combined with point-of-load (POL) dc-dc converters. A higher bus voltage reduces the current for a given power level, which minimizes distribution losses. Google, for example, has proposed such a rack architecture to the Open Compute Project, an industry consortium focused on developing energy-efficient data centers.



1. Generating a 1-V dc supply for a server microprocessor requires multiple ac-dc and dc-dc conversion stages; around 33% is wasted as heat along the way (Source: Texas Instruments)

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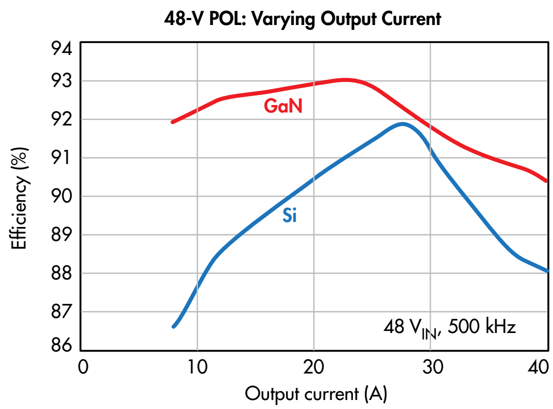
At the dc-dc stages, this is driving the adoption of new semiconductor materials and high-efficiency POL designs that can convert 48 V to 1 V in a single stage.

The Case for Gallium Nitride

For many years, silicon has been at the heart of the vast majority of semiconductor devices. Now, however, gallium nitride (GaN) is replacing silicon as the material of choice for power transistors in industrial automation, motor drivers, high-frequency dc-dc conversion, and similar applications.

Why use GaN? It's one of a class of wide-bandgap (WBG) semiconductors that have superior performance to silicon in power applications. GaN's bandgap energy is 3.4 eV, compared to 1.1 eV for silicon. The higher energy gives GaN power transistors a number of advantages, including:

- Lower gate capacitance and output capacitance for higher switching frequency with lower switching losses.
- Higher efficiency, resulting in lower conduction and switching losses, and low or zero reverse recovery losses.
- A smaller footprint for higher-power-density designs.
- Lower $R_{DS(on)}$ for higher current operation.



2. GaN maintains several advantages over silicon in high-power dc-dc converters, providing an efficiency edge at all load points. (Source: Texas Instruments)

There are other WBG semiconductors, notably silicon carbide (SiC), with a bandgap energy of 3.3 eV. Still, GaN is expected to dominate in high-performance power applications up to about 50 A and 200 V.

In a 48-V POL dc-dc converter, switching from Si to GaN results in an efficiency improvement across the board *(Fig. 2).*

Combine Driver and GaN for Best Performance

Although GaN transistors switch much faster than silicon MOSFETs and can achieve lower switching losses, it's important that the rest of the design helps make the most of these advantages.

GaN devices are typically packaged separately from their drivers because they use different process technologies. Each package can introduce additional parasitic inductance into the circuit from internal bond wires or printed-circuit-board (PCB) interconnects, and this can limit GaN switching performance at high slew rates. Integrating the GaN FET and driver into the same package reduces parasitics and optimizes switching performance.

A single package also makes it easier to include protection features. Overcurrent-protection circuits, for example, require low-inductance connections between the GaN device and its driver. Extra inductance can cause ringing and requires a long blanking time to keep the current protection from misfiring. Integrating the driver minimizes the inductance between the sensing circuit and the GaN FET so that the current-protection circuit can react as quickly as possible.

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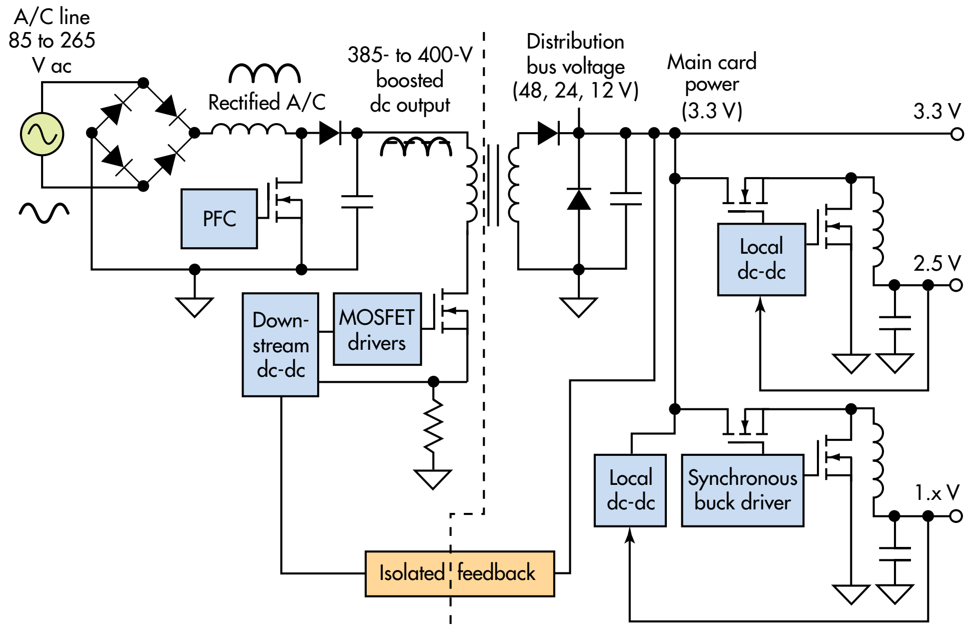
Since the package lead frame is an excellent heat conductor, the temperatures of the driver and GaN FET can track each other closely. Thermal sensing and overtemperature-protection circuits can then be included on the driver chip to protect the FET.

Architectural Benefits of GaN Devices

Using a GaN power stage has architectural advantages, too. *Figure 3* shows the ac-dc and dc-dc stages in the power-conversion chain discussed earlier. The 48-V dc or 12-V dc bus voltage on the secondary side of the isolation transformer is stepped down to an intermediate 3.3 V; then one or more buck converters generate the voltages needed for processors and other components.



3. The secondary side of a typical offline converter uses 48 V as the dc bus voltage, with an intermediate dc-dc stage feeding 3.3 V to additional low-voltage POL converters. (Source: Texas Instruments)

A GaN device allows the design of a single-stage, high-efficiency, 48-V-to-1-V dc-dc converter. The elimination of the intermediate stage saves cost and reduces size at the board level; at the room level, it also reduces cooling costs.

GaN DC-DC Converter Topologies

Several different dc-dc converter topologies can be used to convert 48 V to 1 V, each coming with advantages and disadvantages. The buck converter is perhaps the simplest and lowest cost, but has lower efficiency. The transformer-based half-bridge topology, on the other hand, is considerably more complicated and offers higher efficiency at a higher cost.

The half-bridge topology efficiently supports a high step-down ratio while providing fast transient response and significant output current courtesy of the full-wave rectifier on the secondary side of the transformer. Let's look at a half-bridge design example in more detail.

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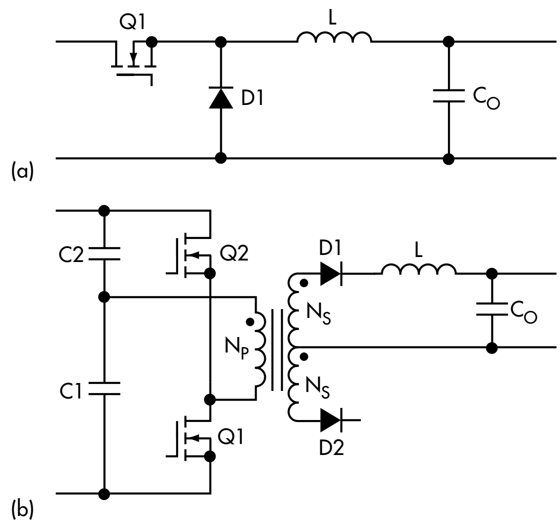


4. The simple buck (a) and the half-bridge dc-dc converter (b) topologies emphasize low cost and high performance, respectively. (Source: Texas Instruments)

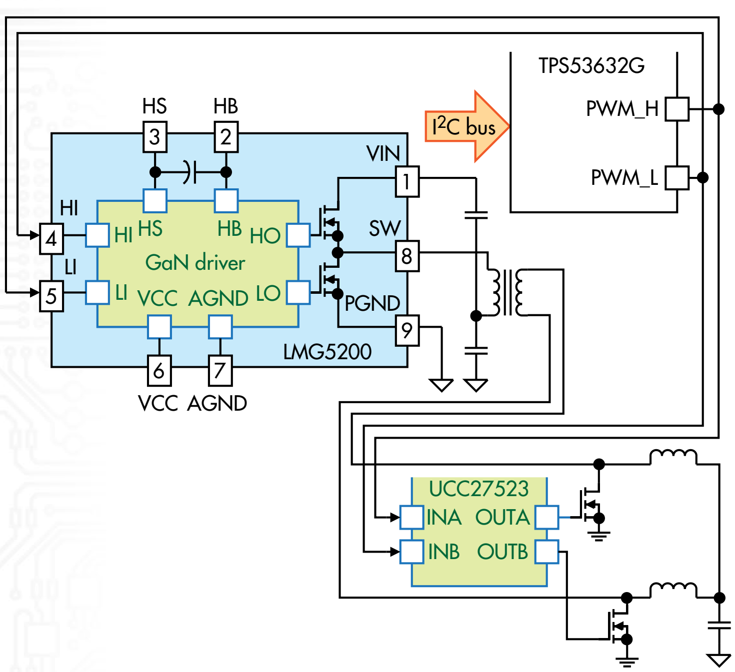
Application Example

Figure 5 shows the block diagram of an efficient 48-V/1-V POL converter design using the LMG5200 80-V, 10-A GaN half-bridge power stage, and the TPS53632G half-bridge POL controller.

The LMG5200 provides the primary-side FETs Q1 and Q2 in Fig. 4b. It integrates two 18-mΩ GaN FETs and their driver into a single device. To minimize parasitic inductances, all three devices are mounted in a nine-pin QFN package that contains no bond wires.

The TPS53632G controller uses a D-CAP+ hysteretic control architecture and features Valley Current Mode with adjustable ON time control, adjustable slew rate, and fast transient response. The part can switch up to 1 MHz when paired with a suitable GaN power stage. An I^2C Rev 3.0 interface enables output voltage control and feeds back current-monitoring information.

The secondary side includes a current-doubler rectifier, a refinement of the full-wave rectifier shown in Fig. 4b. In this configuration, the transformer secondary isn't center-tapped; instead, there are two inductors, each carrying half of the dc output current. This arrangement adds complexity, but simplifies the power transformer design, dissipates less power, and requires smaller magnetic components.



To further increase efficiency and lower power dissipation, a UCC27523 dual low-side MOSFET driver and two EPC2023 GaN FETs replace the diodes to add synchronous rectification to the current-doubler circuit. The TPS53632 provides the drive signals for the UCC27523.

Although this design is non-isolated, an isolated version can be imple-

5. Shown are key components of a GaN-based non-isolated 48-V/1-V dc-dc converter. The design uses the LMG5200 GaN power stage, the TPS53632 half-bridge PWM controller, the UCC27523 dual-MOSFET driver, and two discrete EPC2023 GaN FETs. (Source: Texas Instruments)

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mented by adding a digital isolator such as the ISO7820 between the TPS53632 and the primary-side devices.

The LMG5200POLEVM-10A evaluation module (EVM) is available to evaluate this design. The user manual includes the complete schematic, which supports input voltages from 36 to 75 V and output voltages from 0.5 to 2.5V.

Layout Guidelines

As discussed earlier, it's important to optimize all aspects of the design to take full advantage of GaN technology, and no more so than in the PCB layout.

Reducing parasitic capacitance is particularly critical. For example, it's vital to minimize any capacitance from the switching node to ground or VIN. Any parasitic capacitance must be charged during FET turn-on, which increases switching losses. It's also important to pay attention to interlayer capacitance in multilayer boards. Even heat sinks with insulated thermal interfaces can add parasitic capacitance.

Interference is another issue to be managed. High-power GaN switching can interfere with low-level logic devices, and poor layout can cause a range of undesirable effects ranging from inadvertent turn-ons to shoot-throughs and false triggers.

GaN layout guidelines are covered in more detail in TI's application note SNOA946, which discusses another half-bridge GaN design, this one using the LMG3410 600-V, 12-A Smart GaN power stage.

Conclusion

GaN transistors offer key advantages to designers of low-voltage, high-current POL converters for telecom and server applications. To make the most of their performance, though, it's necessary to pay attention to some key design guidelines.

TI has a range of GaN solutions, evaluation boards, application notes, and tools that cover these areas and help engineers develop a successful design.

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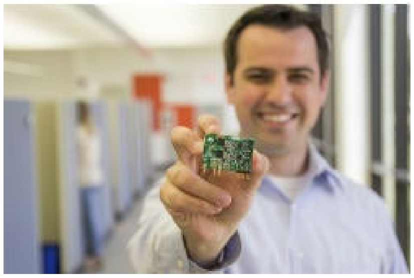

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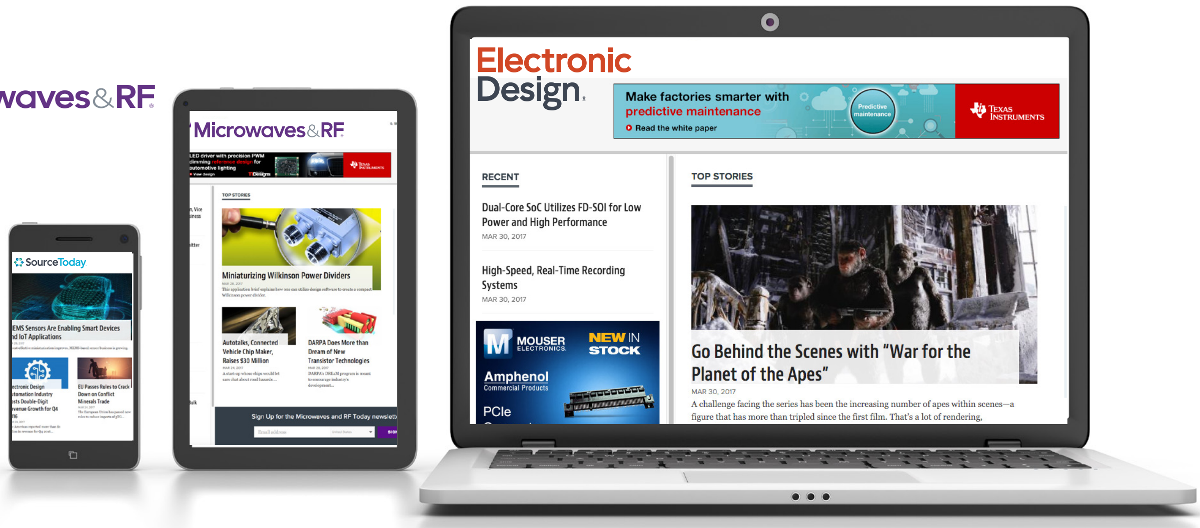

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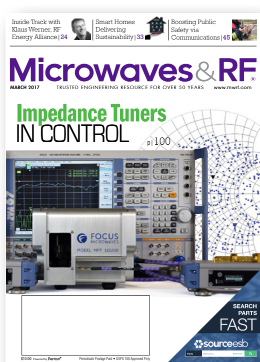

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